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GAL Sourcecode made and tested with the GDSWin GAL-Compiler from SH-Elektronik Kiel

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/\* Version 1.0 form 07.19.2008
The GAL22V10 Logic is create for the 512k memory extension.
under the TAPR\_Open\_Hardware\_License\_v1.0

Switch position

512k Rambo extension SW1=on SW2=on
256k Rambo extension SW1=on SW2=off
256k CompyShop extension SW1=off SW2=on
Memory extension off SW1=off SW2=off \*/

CHIP SRAM\_512k GAL22V10 REGISTERED\_MODE

/\*1 2 3 4 5 6 7 8 9 10 11 12\*/
CLK HALT PB4 PB5 PB7 RW PHI2 CI\_IN PHI0 A14 A15 GND

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NC SW1 SW2 MHALT CI\_OUT MAP A16A A18A RWOUT CE PHI2N VCC
/\*13 14 15 16 17 18 19 20 21 22 23 24\*/

/\* PHI2 must negativ to create the CLK signal for the GAL. If the PHI2 signal goes down then the HALT Signal will be latched. This takes U35 one 74 LS95B shift registers, look in this, at the 130 XE Wiring diagram of the 130 XE. \*/

PHI2N = /PHI2;

/\* The hold signal is taken on by PHI2 only at falling flank. A positive drive since but CLK needs one must negate the PHI2 signal before. The signal at the exit is only internally processed \*/
MHALT := HALT;

/\* Turns the internal memory of the computer off if the expansion is active
CAUTION: By a negative logic an OR becomes this one AND combination! \*/

CI\_OUT = CI\_IN & CE;

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/\* Supplementary memory switched off selftest" \*/
/ MAP = PB4 & /PB7;
A16A = PB5 & SW1; /\* 256k RAM CompyShop at SW1 on and SW2 off active \*/
A18A = PB7 & SW2; /\* 256k RAM Rambo at SW2 on and SW1 off active \*/

/\* The Write signal connects PHI2 and PHI0 with system time.
PHI0 so that the write access ends before the signal PHI2 and a safe degree takes place \*/

/RWOUT = PHI0 & PHI2 & /RW;

/\* The conditions concerning the activation RAM
Memory \$4000-\$7FFF (A14=1 and A15=0) select and
PB4=0 (memory extention on) and
switch position SW1+SW2=1 or SW1=0 + SW2=1 or SW1=1 and SW2=0
PB4=0 memory on \*/

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/CE = A14 & /A15 & /PB4 & SW1 & SW2 /\* 512k extendet Mem Type "Rambo" on \*/
+ A14 & /A15 & /PB4 & SW1 & /SW2 /\* 256k extendet Mem Type "Rambo" on \*/
+ A14 & /A15 & /PB4 & /SW1 & SW2 & MHALT /\* 256k extendet Mem Type "Compysop" on \*/
+ A14 & /A15 & /PB5 & /SW1 & SW2 & /MHALT; /\*256k Antic Zugriff Type "Compysop" on \*/

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